Silicon Mobility
535 Route des Lucioles
Les Aqueducs – Bâtiment 2
06560 Valbonne /
Sophia Antipolis France

Location: Sophia-Antipolis, France
Employment type: Experienced Professional
Contract type: Permanent position

Ref: RD_SIPV_ENG

SOC/IP VERIFICATION MANAGER

The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, connectivity are trends that are drastically changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to support the rapid advent of electric and hybrid cars.

Silicon Mobility, an Intel company, is a technology leader for cleaner, safer and smarter mobility. The company designs, develops and sells flexible, real-time, safe and open semiconductor solutions named FPCU (Field Programmable Control Unit) for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe.

The Company is opening an **"SoC/IP Verification Manager"** position in its main Research and Development center ideally located in the Sophia-Antipolis Technology Park on the French Riviera.

You are a brilliant and passionate SoC/IP Verification for System on Chip for Automotive Applications? You want to support the development of disruptive products accelerating the car powertrain electrification? At Silicon Mobility, we like to light up our employees' potential. Are you up for the challenge? Contact us and send your resume and cover letter to **recruitment@silicon-mobility.com**

ROLE & MISSIONS

As part of the FPCU IC Engineering team, you will work on front-end design verification activities.

Primary responsibilities of the position are:

- IP/SoC verification organization and strategy
- Management of a team of IP/SoC verification engineers (internal or external):
  - Participate in team staff recruitment (internal or external).
  - Define the tasks and objectives.
  - Follow the tasks execution.
- IP/SoC Verification tasks expert:
  - Review IP/SoC Top Level Test Plan definition
  - Review IP/SoC Top Level Test Plan implementation
  - Support Test execution, debug and coverage.
  - SoC top level verification in simulation, FPGA, hardware accelerator …
  - SoC top level verification at RTL and gates level.
- Lead the Functional Safety (ISO26262) verification at IP level and SoC top level including the fault simulation campaign.
- Management of Verification tools (main interface with EDA provider for Verification tools).
- Development of Verification design flow automation scripts.
- Verification technology intelligence: methodology and tools.

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REQUIRED SKILLS AND EXPERIENCE

EDUCATION:

- Good university degree in microelectronics engineering

TECHNICAL SKILLS & EXPERIENCE:

- A minimum of 15 years of experience in IP/SoC Verification.
- Strong experience in SystemVerilog and UVM verification.
- Strong Experience in Verilog/VHDL RTL.
- Experience in oriented object programming and C/C++ language.
- Experience in team management and/or task subcontracting.
- Good knowledge of SoC architecture and ARM Amba AXI/AHB/APB bus protocol.
- Good knowledge in scripts writing (Makefile, Shell, Perl,…).
- Knowledge of Siemens/Synopsys/Cadence EDA tools is highly recommended.
- Experience in functional safety ISO26262 will be appreciated.

LANGUAGE SKILLS:

- Fluent in English

BEHAVIORAL SKILLS:

- Be self-motivated, pro-active, flexible and capable of accepting new challenges.
- Be autonomous, organized, rigorous, and have a high sense of priorities.
- Demonstrate strong communication skills at technical and management levels.
- Be able to work efficiently across different teams within Silicon Mobility to understand their individual needs and constraints.