Silicon Mobility
535 Route des Lucioles
Les Aqueducs – Bâtiment 2
06560 Valbonne /
Sophia Antipolis France

Location: Sophia-Antipolis, France
Employment type: Experienced Professional
Contract type: Permanent position

Ref: HW_SDFT_ENG

SOC DFT ENGINEER

The Automotive industry is living a revolution. Electrification, autonomous driving, diverse mobility, connectivity are trends that are drastically changing the industry's rules. Among all decisive topics revolutionizing cars in the next future, Silicon Mobility is committed to support the rapid advent of electric and hybrid cars.

Silicon Mobility, an Intel company, is a technology leader for cleaner, safer and smarter mobility. The company designs, develops and sells flexible, real-time, safe and open semiconductor solutions named FPCU (Field Programmable Control Unit) for the automotive industry used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe.

The Company is opening an **"SoC DFT Engineer"** position in its main Research and Development center ideally located in the Sophia-Antipolis Technology Park on the French Riviera.

You are a brilliant and passionate System on Chip Design For Test (DFT) design for Automotive Applications? You want to support the development of disruptive products accelerating the car powertrain electrification? At Silicon Mobility, we like to light up our employees' potential. Are you up for the challenge? Contact us and send your resume and cover letter to **recruitment@silicon-mobility.com**

ROLE & MISSIONS

As part of the FPCU IC Engineering team, you will work on DFT activity under the responsibility of the DFT manager.

Primary responsibilities of the position include:

- DFT implementation at SoC level including Logic (Scan and LBIST), Memories (MBIST), Analog function.
- DFT verification at RTL and gate level.
- DFT coverage analysis.
- Production test generation and test.
- Production test implementation support.

The position requires pro-active involvement with the whole SoC development team.

REQUIRED SKILLS AND EXPERIENCE

EDUCATION:

- Good university degree in microelectronics engineering

TECHNICAL SKILLS & EXPERIENCE:

- A minimum of 5 years of experience in SoC Design For Test (DFT)
- Very good knowledge of the DFT tools (Scan, MBIST, Test pattern generation, …).
- Good knowledge of SoC architecture and ARM Amba AXI/AHB/APB bus protocol.

- Good knowledge in scripts writing (Makefile, Shell, Perl,…).
- Knowledge of Siemens Tessent EDA tools is highly recommended.
- Experience in production test implementation is appreciated.
- Experience in functional safety ISO26262 will be appreciated.
- Knowledge in cybersecurity will be appreciated.

LANGUAGE SKILLS:

- Fluent in English

BEHAVIORAL SKILLS:

- Be self-motivated, pro-active, flexible and capable of accepting new challenges.
- Be autonomous, organized, rigorous, and have a high sense of priorities.
- Demonstrate strong communication and team working skills.