OLEA® U310

A single chip solution for highly integrated powertrain domain control and energy management

Top notch FPCU technology

- **AxEC[1]:** Hard real-time control on mutliple parallel applications with flexible hardware
- **SiLant[2]:** Safe multi-core & processing clusters with guaranteed worst case execution time
- **FHSM[3]:** Cybersecure with flexible hardware security module to support current and future threats
- **ISO 26262 ASIL-D & ISO/SAE 21434** compliant

All-in-one capabilities for EV power and energy control

The OLEA U310 is a new addition to Silicon Mobility FPCU portfolio and has been engineered to match the need for powertrain domain control in electrical/electronic architectures with distributed software. The OLEA U310 is built with a unique hybrid and heterogenous architecture embedding multiple software and hardware programmable processing and control units seamlessly integrating functional safety and cybersecurity into its core design, surpassing the capabilities of traditional microcontrollers. It hosts and bridges in one chip the time-based and multi-task software application needs with the critical event-based multi-functions control requirements.

Design your E-powertrain function grouping

The OLEA U310 chip simplifies complex system design by replacing up to 6 microcontrollers and efficiently controlling multiple functions in parallel, including inverters, motors, gearboxes, DC-DC, OBC, Auxiliary Functions and more. Here are some example of use cases.

All-in-1 Powertrain System

Four real-time function control

- Inverter and motor
- OBC (PFC + DC/DC HV-HV Converter)
- DC/DC HV-LV Converter
- Auxiliary Function

Dual Motor Control

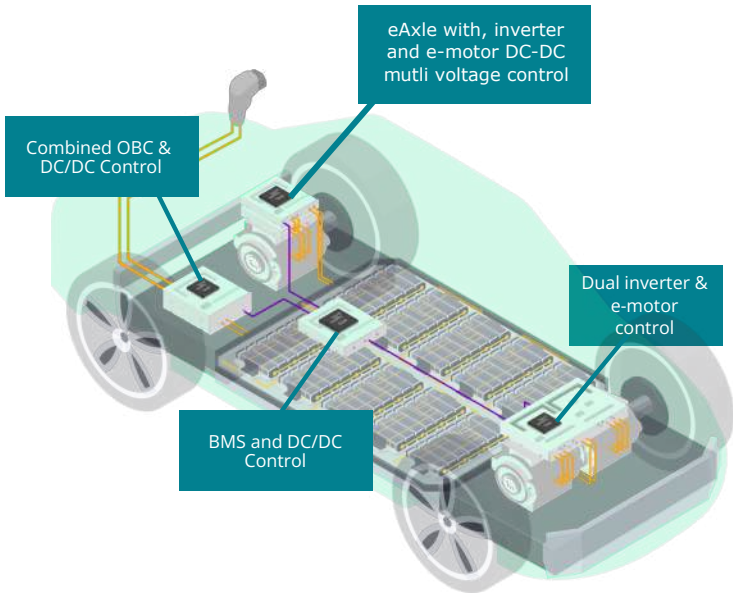
Two real-time function control

- First inverter and motor
- Second inverter and motor

Power & Energy Management

Four real-time function control

- OBC (PFC + DC/DC HV-HV Converter)
- DC/DC HV-LV Converter
- Battery Management System

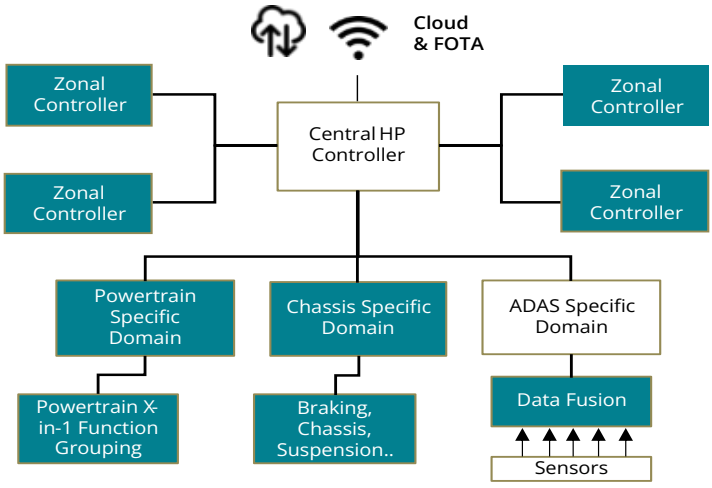


Design for the latest automotive control needs

The OLEA U310's capabilities extend beyond powertrain. This versatile system-on-chip can also be used for:

- Chassis Control Systems
- Data Fusion
- Air compressor
- Thermal Management System
- Other Control Systems

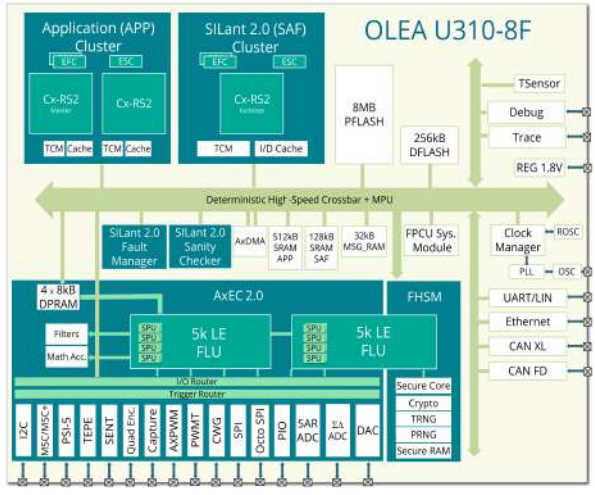
By leveraging the OLEA U310's versatility, EV manufacturers can achieve a more integrated and efficient control system, leading to improved control & performance.



Key technologies at the heart of OLEA U310

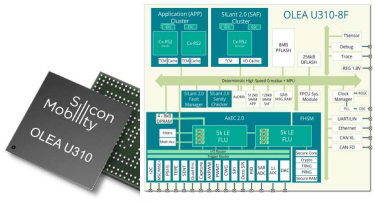
Key Features

- 2nd generation of FPCU
- 3x Cortex-R52 @ 350MHz – 2196 DMIPS
- AxEC 2.0: 2x FLUs @ 175Mhz – 400 GOPS + 9.1 GMAC
- SILant 2.0: Safe and Determinist Multi-Core/FLU
- Flexible HSM: HW & SW EVITA Full
- 8MB of P-Flash, 256kB of D-Flash, 1MB of SRAM
- CAN FD, CAN XL, Ethernet
- ISO 26262 ASIL-D & ISO/SAE 21434 compliant
- AEC-Q100 Grade 1
- 292 BGA



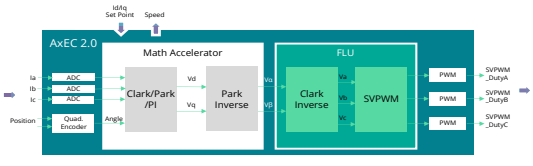
With unprecedented performances

Massive Parallel Data Processing



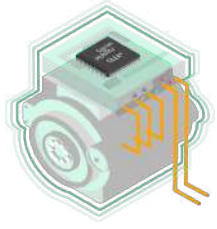
Max Clock Speed: 350 MHz
CPU Processing Speed: 2194 DMIPS
AxEC Math Acc.Speed: 400 GOPS
AxEC SPU Processing Speed: 9.1 GMAC
AES_CMAC Decryption: 91 MB/s

Fast & Precise Parallel Real-Time Control



PWM Min Resolution: 180 ps
PWM Max Freq.switching: 175 MHz
Inverter Control:
Max Freq. FoC Loop: 1 Mhz
Nb of parallel FoC at Max Freq: 4x
Power Factor Corrector:
Max Freq. Loop: 1 us / 1Mhz
DC/DC PSFB:
Max Freq. Loop: 1 us/Mhz
Max Phases at Max Freq: 8x

Optimized System Efficiency and Integration



Ex: Optimized Pulse Pattern:
Efficient Improvement: +5%
Motor Downsizing: -25%
Cooling Need Reduction: -35%
DC-link Capacitor downsizing: 30x less

Digital Control Integration:
1x OLEA U310 FPCU=
4x Real-time 32b MCU +1xFPGA

What is an FPCU?

OLEA U310 is based off the FPCU architecture. It is an hybrid architecture made of two type of processing units:

1. It embeds standards ARM CPU cores which runs the software. The cores are split into an application custer and a safety dedicated cluster.

2. It is powered by AxEC, a data processing and real-time control unit based on programmable hardware. It integrates mathematical accelerators and configurable peripherals supporting multiple parallel applications execution thanks to multi-FLU (Flexible Logic Units) clusters.

About the AxEC[1]

The Advanced eXecution and Events Control (AxEC) is composed of a:

- Flexible Logic Unit, or FLU, which integrates LUT, FF and 32-bit Signal Processing Units.
- Set of peripherals which are configurable via registers accessible by the FLU or the CPU cores. These peripherals are used to interface the FPCU with actuators and digital or analog sensors.
- Mathematical accelerator units which multiply the data processing capabilities of the AxEC.

The FLU, Peripheral and I/Os of the AxEC are surrounded by an extensive triggers routing system. Once configured, a series of chained actions can be automatically launched as a response to specific events, requiring zero software intervention and processed in parallel to each others.

To interact with the AxEC, the CPU cores can exchange data using a Dual Port RAM directly or using a Safe DMA. Both the CPU cores and AxEC can generate interrupts toward each other for synchronization.

Key Highlights

Flexible Logic Unit

- Spatial segregation for safe applications parallelization
- Virtualization
- Multiple clock domains
- Internal SRAMs
- SPUs

Signal Processing Unit

- 32-bits or 2 x 16-bits processing
- 2 clock domains
- Single precision FP support

Mathematical HW operators

- 32-bits operators on divider and square root
- Matrix multiplication
- PID features
- Multi-point linear interpolator in floating point

About the SiLant[2]

The Safety Integrity Level agent (compliant to ISO 26262) is a set of unit and functionalities dedicated to the FPCU and the system functional safety. This new generation has a deterministic multi-core and multi-FLU cluster and guarantees worst-case execution time

Key highlights

Deterministic Architecture

- Guaranty of WCET
- Each CPU has its exclusive memory
- Deterministic crossbar with multiple priority type management

Safe Multitasking

- Unified firmware virtualization from CPU down to FLU level
- FLU matrix physical partitioning for multi-tasking independency

Fail Safe FLU

- Triplication of all FFs
- Fast bitstream fault detection in less than 100ns
- Parity bit protection on SRAM
- Temporal and spatial redundancy safety mechanism

About the FHSM^3

The Flexible Hardware Security Module is an EVITA Full & ISO-21434 sub-system dedicated to the cybersecurity of the FPCU integrating encryption/decryption accelerators and identification key management. It is combined with a hardware programmable cluster enabling to support yet unidentified threats and strengthen security.

Main Features

AxEC Peripheral	48-ch/24-ch PWMT/inc. HRPWM 8-ch Complex Waveform Generator 1x TEPE (Thermal Engin Position Estimator) 2x QENCODER 10-ch CAPTURE/COMPARE 10x SENT 3x PSI-5 64-ch I/O Dgital Filter 18-ch ANALOG COMPARE (2 compare/channel) 64-ch* 12-bit SAR ADC @4MS/sec 2-ch 16bit SD ADC @ 330kS/sec 2-ch 12-bit DAC / Soft Switching support 2x 16-ch Integrated DMA in lockstep
AxEC Math Accelerator	5x MCR (MM, CORDIC, 2 xPID) + CORDIC 2x DIV, SQRT, 6x6 MULT 2x Interpolator 4x FIR 8-order 4x IIR 4-order 2x De-modulator
SiLant	3x EFC - Multi-Core Determinist 4x ESC + FLU Programming Protection + FLU Incremental Design + Virtualization support + PWM and DMA in LS + ECC end 2 end + Configuration registers + I/O, clock, resets, supply
FHSM	350MHz 32-bit CPU + EVITA FULL inc. OSCCA & NIST + FLU
Multi-Core	350 MHz Cortex-R52 2/1LS + 1LS CPU organization + FPU 2195 DMIPS
Memories	8 MB NVM 1 MB SRAM (+TCM & Cache) 256 kB Data flash (with FPU prog.)
AxEC FLU	4 x 8kB / 64-bit DPRAM Size/Data width 2x16-ch Direct Read Channel to Peripheral (DRC2PRP) 2x2ch Direct Read Channel to FLU 2x 64-bit + Buffered HS Master Interface (MIF) 2x 32-bit + Buffered Slave interface (SIF) 1 x 64-bit Programing I/F (PIF) 10k Logic Elements (LE) 2x LE FLU partition 52x SPU 16-bit/32-bit SPU data width 230 kbit integrated RAM 150 MHz Clock Frequency 4 Clock Rate domains 150 kB Bitstream size
Communication Ports	4x/1x CAN-FD/XL 1x 10M/100M/1Gbit/s Ethernet 3x Master/Slave SPI 1x Master/Slave Octal-SPI 4x UART-LIN 2.3 2x I2C 3x MSC (2 MSC-plus + 1 MSC)
Debug Calibration	1x / 1x JTAG / SWD + High-speed TRACE + 16-ch AxEC Signal Trace + Calibration
System	2x 16-ch DMA in Lockstep 3x WatchDog 2x CRC
I/Os Supply Package Power	3.3V I/O 1.8V/ 3.3V I/O 136 PIO +48/+4 ANIN/ANOUT +20 ANIN/DIN multiplexing 3.3V/1.0V CORE Supply BGA 292 Packages 40°C to +125° Temperature (Ambient) 850 mA Consumption @ 350Mhz, Tj=150°C

Available development tools and software

OLEA® U310 Eval. Board

OLEA® COMPOSER

OLEA® LIB

www.silicon-mobility.com
sales@silicon-mobility.com
535 Route des Lucioles
Les Aqueducs – Bâtiment 2
06560 Sophia Antipolis
France

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